Appl. No. 10/075,356 Amdt. Dated Feb. 20, 2004 Reply to Office Action of Nov. 20, 2003

Amendments to the Specification

Please insert a new paragraph after paragraph [0019] as follows:

[0019.1] FIG. 9 is a plan view of an intermediate layer of the printed circuit board, wherein traces extending from footprints T1, R1, T2, R2, T4 and R4 are omitted for clearly showing continuous traces extending from T3 and R3.

Please amend paragraph [0020] as follow:

Referring to FIGS. 1, 3 and 3 9, the medial traces 5 connect [0020] connected to a chosen pair (T3, R3 for example) are used to compensate the pair to pair noise which arises in electrical devices like cables or electrical connectors due to their parallel arranged conductors. The trace connected to the conductive footprint T3 extends from the corresponding metalized hole 4 and then extends down two-layers one layer, back under itself, via the dotted lines T3', under the footprint R2, and continuing on to C3' C3. The trace connected to the footprint R3 extends from the end of a corresponding metallized hole 4 and then extends down one layer two layers, back under itself, via the dotted lines T3' R3', under pad T2, and continuing on to C3 C3'. C3 and C3' are then a coupled differential pair running down the length of the PCB. The corresponding footprint R3', T3' connected to the chosen pair R3, T3 is parallel to the footprint of the adjacent pair T2, R2 and signals passing through the footprints T2, R2 can be compensated due to coupling with the footprints T3, R3', R3, T3' of the chosen pair at the same time. It is understandable that only the neighborhood area of the footprints 2 is occupied by compensating circuits. And the predetermined length of every footprint 2 needed to connect to the corresponding conductors of the electrical devices is long enough for better compensating performance. Therefore space-saving and miniaturization of a built-in printed circuit board can be easily achieved.

[0022] Referring to FIGS. 4 and 5, a second embodiment of the printed circuit board in accordance with the present invention is shown. An enlarged footprint R3", T3" T3", R3" instead of the footprint R3', T3' T3', R3' having the same size as footprint 2 is respectively formed along the traces C3, C3' on intermediate layers 12 which are connected to the chosen pair T3, R3 and detoured to pass through a corresponding area next to footprints 2 of the

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adjacent pair T2, R2 R2, T2. Better electrical performance will be achieved because a larger coupling area is available respectively with the enlarged footprint R3", T3" and the adjacent pair T2, R2 to assure of complete noise compensation.

Referring to FIGS. 6 and 7, a third embodiment of the printed circuit [0023] board in accordance with the present invention is shown. The trace C3 on the intermediate layer 12 right next to the upper face 11 of the substrate 10 has a compensating footprint R3' T3' formed on the corresponding parallel area of the intermediate layer 12 to one of the footprints 2 of the pair T2, footprint R2 on the upper face 11, and the compensating footprint R3' T3' has the same size as its coupling footprint T2 of the pair T2, R2. Besides, the trace C3', which is on the intermediate layer 12 right next to the lower face 13, has an enlarged footprint T3" R3" formed on the corresponding parallel area of this intermediate layer 12 to the other footprint R2 T2 of the pair T2, R2. The size of the compensating footprints R3' R3" and T3" T3' is decided by the distance between the intermediate layers 12 they are mounted and the upper face 11 where their coupling paired footprints T2, R2 are mounted. The coupling footprints R2, T3" T2, R3" having a larger distance therebetween are designed to have an enlarged compensating footprint T3" R3". Better electrical performance than fore-mentioned two embodiments will be achieved while not only a larger coupling area is available from the enlarged footprint T3" R3" and its coupling footprint R2 T2 but also a new balance of signal compensation between these coupling pair R2, T3" T3' and T2, R3" will be established.